**SUMMARY:**

This lab focuses on basic digital circuits including both non-inverting and inverting logic gates. The purpose of this lab is to test and analyze different logic gates in both separate and combined circuits including a 1-bit full adder. To validate the results, observations are compared with truth tables for each circuit and checked against prior hypotheses. This lab showcases the differences between different logic gates and how the truth tables can be used to predict the outcomes of basic binary operations. This lab also looks at the differences between the ideal voltages associated with the logic levels, and their actual counterparts. The outcomes of this lab are exactly as expected, and the hypotheses are proven to be justified.

**INTRODUCTION:**

Today, most devices and machinery have embedded systems at the core of their operations. From microwaves to automobiles, digital circuits run simple to highly complex functions such as timing to automation. In order to design such systems a strong foundation in basic digital circuits and components is required. The purpose of this laboratory is to get a basic idea of some integrated circuits (IC’s) and their functionality. The IC’s that are focused on within this lab are digital logic gates. The logic gates are both non-inverting, such as AND, OR, and XOR, as well as inverting, such as NOT, NAND, NOR, and XNOR. With these basic IC’s simple and even some complex operations can be completed.

The ideas focused on in this lab are testing and understanding the IC’s previously mentioned, and designing a basic digital circuit known as a 1-bit full adder. In order to better understand what each of these logic gates does the use of truth tables will be employed. Truth tables are tables which showcase the outputs from the logic operations based on their binary inputs. These tables compile all the possible outcomes that can occur from various inputs. Some logic gates are 2-bit inputs (a and b), and others are 3-bit inputs (a, b, and carry-in) with the outputs respectively being either 1-bit (y), or 2-bit (y and carry-out). With this basic understanding, further advancement into more complex IC’s can be attained.

**PRE-LAB DISCUSSIONS:**

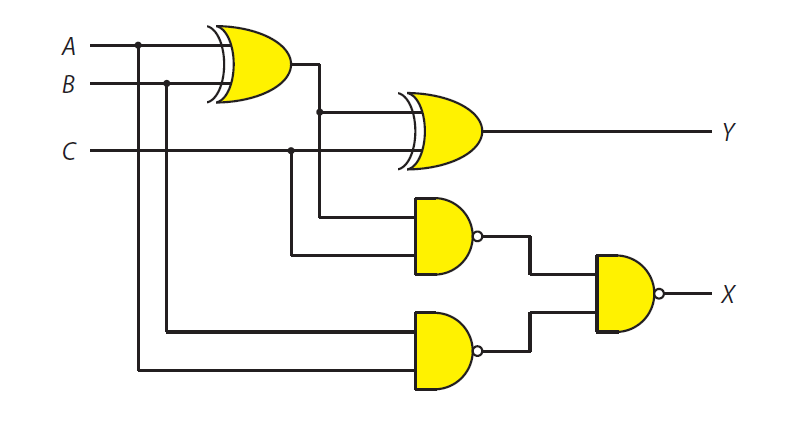
The following are the truth tables used in this lab:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **AND** | | |  | **OR** | | |  | **XOR** | | |
| **a** | **b** | **y** |  | **a** | **b** | **y** |  | **a** | **b** | **y** |
| 1 | 0 | 0 |  | 1 | 0 | 1 |  | 1 | 0 | 1 |
| 0 | 1 | 0 |  | 0 | 1 | 1 |  | 0 | 1 | 1 |
| 1 | 1 | 1 |  | 1 | 1 | 1 |  | 1 | 1 | 0 |
| 0 | 0 | 0 |  | 0 | 0 | 0 |  | 0 | 0 | 0 |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **NAND** | | |  | **NOR** | | |  | **XNOR** | | |
| **a** | **b** | **y** |  | **a** | **b** | **y** |  | **a** | **b** | **y** |
| 1 | 0 | 1 |  | 1 | 0 | 0 |  | 1 | 0 | 0 |
| 0 | 1 | 1 |  | 0 | 1 | 0 |  | 0 | 1 | 0 |
| 1 | 1 | 0 |  | 1 | 1 | 0 |  | 1 | 1 | 1 |
| 0 | 0 | 1 |  | 0 | 0 | 1 |  | 0 | 0 | 1 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **NOT** | |  |  | **1-Bit Full Adder** | | | | |
| **a** | **y** |  |  | **a** | **b** | **c** | **y** | **x** |
| 1 | 0 |  |  | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 |  |  | 0 | 1 | 0 | 1 | 0 |
|  |  |  |  | 0 | 0 | 1 | 1 | 0 |
|  |  |  |  | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  | 1 | 0 | 1 | 0 | 1 |
|  |  |  |  | 0 | 1 | 1 | 0 | 1 |
|  |  |  |  | 1 | 1 | 1 | 1 | 1 |
|  |  |  |  | 0 | 0 | 0 | 0 | 0 |

This is a diagram for the 1-Bit Full Adder designed in this lab:



**74LS00**

**74LS00**

**74LS00**

**74LS86**

**74LS86**

**3y**

**3b**

**3a**

**2y**

**2b**

**2a**

**1y**

**1b**

**1a**

**2y**

**1y**

**2b**

**2a**

**1b**

**1a**

Figure

**EXPERIMENTAL OBSERVATIONS:**

**Basic Gates:**

Below are the measured truth tables for each of the IC’s tested:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **74LS08 (AND)** | | |  | **74LS32 (OR)** | | |  | **74LS86 (XOR)** | | |
| **a** | **b** | **y** |  | **a** | **b** | **y** |  | **a** | **b** | **y** |
| 1 | 0 | 0 |  | 1 | 0 | 1 |  | 1 | 0 | 1 |
| 0 | 1 | 0 |  | 0 | 1 | 1 |  | 0 | 1 | 1 |
| 1 | 1 | 1 |  | 1 | 1 | 1 |  | 1 | 1 | 0 |
| 0 | 0 | 0 |  | 0 | 0 | 0 |  | 0 | 0 | 0 |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **74LS00 (NAND)** | | |  | **74LS02 (NOR)** | | |  |  | | |
| **a** | **b** | **y** |  | **a** | **b** | **y** |  | **74LS04 (NOT)** | |  |
| 1 | 0 | 1 |  | 1 | 0 | 0 |  | **a** | **y** |  |
| 0 | 1 | 1 |  | 0 | 1 | 0 |  | 1 | 0 |  |
| 1 | 1 | 0 |  | 1 | 1 | 0 |  | 0 | 1 |  |
| 0 | 0 | 1 |  | 0 | 0 | 1 |  |  |  |  |

All the measured logic outputs were the same as expected and when compared to the pre-lab truth tables above, they are shown to be the same. The IC’s are in working order and function as expected.

When measuring the logic output for the **74LS266 (XNOR)** gate it first appeared to be malfunctioning for it constantly gave an output of logic-0 even when it should have given an output of logic-1 according to the previously mentioned truth table. This occurred because for that type of logic gate, known as an **open-collector gate**, its physical operation is different from regular logic gates. For logic-0 it gives an output of 0V like a regular gate, but for logic-1 it is incapable of giving power. This is because it essentially acts like an open circuit and as such the voltage may be there, but the impedance theoretically seen as being infinite. So in order to get it to function as if it was powered, a connection must be made between the Vcc and the Vout with a resistor.

In this lab a **1kΩ resistor** is used as the connection. This form of connection is called a **pull-up resistor** and allows the current to take the path of least resistance which allows the gate to function normally because **1000 < ∞** so that when the gate becomes an open circuit, current flows through the resistor (thus logic-1), but when the gate isn’t an open circuit then the path of least resistance is not the resistor but instead through the IC, leading to an output of logic-0.

**Voltage vs. Logic Levels:**

In order to analyze the difference between actual and ideal voltages representing the logic levels of an IC a potentiometer was used to adjust the voltage (by changing the resistance) at V­­­in on the IC, and then measuring the output Vout it is possible to see the real voltage associated with logic values.

When Vin is set to approximately 5V (logic-1) on the 74LS04 (NOT) gate, the output V­out was measured to be 0.13V which is the actual voltage associated with logic-0.

Vin = 5.05V Vout = 0.13V

When Vin is set to approximately 0V (logic-0) on the 74LS04 (NOT) gate, the output Vout was measured to be 4.48V which is the actual voltage associated with logic-1.

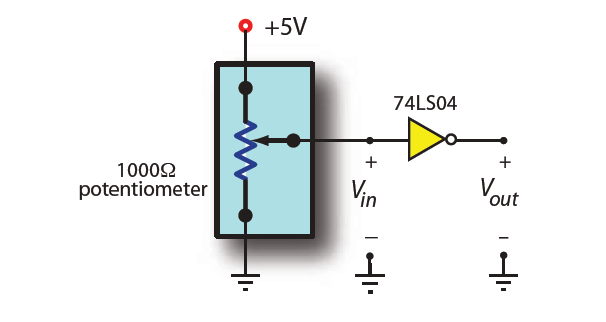
Vin = 0.75V Vout = 4.48V

After the actual voltages were measured, the output was then hooked up to an LED in order to measure what the **threshold voltage** is for the IC. The potentiometer is adjusted so that Vin gradually increases until the LED light goes out.

The threshold voltage was measured to be around 1.015V on the 74LS04 IC.

Vin = 1.015V

Below is a diagram of the circuit used to test for actual logic level voltages:



Figure

**Floating Inputs:**

This experiments looks at the idea of floating inputs which is when one input is left disconnected from the circuit. Below are the observations made when the 74LS02 and 74LS00 are connected via only one input and their output is sent to an LED.

For the 74LS02 IC the following was observed:

Inputting logic-1 led to an output of logic-0.

Inputting logic-0 led to an output of logic-0.

For the 74LS00 IC the following was observed:

Inputting logic-1 led to an output of logic-0.

Inputting logic-0 led to an output of logic-1.

Based on the above observations and relating the outputs to the truth table outputs it appears that a floating input acts like a logic-1 input, so it is predicted that using a 74LS86 (XOR) gate with a floating input, that the following would be observed:

Inputting logic-1 would give an output of logic-0.

Inputting logic-0 would give an output of logic-1.

The idea of floating inputs is an interesting one because it can be used in designs where one input is always expected to be true, and this could be achieved without having to supply the power to one of the inputs. But is also allows IC’s to function as other IC’s with different functionality. So having floating inputs is definitely something that would be beneficial in some designs for example checking if a button is pressed or not.

**1-Bit Full Adder:**

This experiment focused on building a simple 1-bit full adder based on “figure 1” found above in the pre-lab section. After building the circuit all eight different combinations were tested and their outputs observed. Below are the observations made using the circuit:

a = 1 b = 0 c = 0 gave the output: y = 1 x = 0

a = 0 b = 1 c = 0 gave the output: y = 1 x= 0

a = 0 b = 0 c = 1 gave the output: y = 1 x = 0

a = 1 b = 0 c = 1 gave the output: y = 0 x = 1

a = 0 b = 1 c = 1 gave the output: y = 0 x = 1

a = 1 b = 1 c = 0 gave the output: y = 0 x = 1

a = 1 b = 1 c = 1 gave the output: y = 1 x = 1

a = 0 b = 0 c = 0 gave the output: y = 0 x = 0

All the above observations match the truth table shown above in the pre-lab section. The circuit did in fact work as expected and provided the correct output for all eight different combinations.

**CONCLUSION:**

The experiments performed in the laboratory confirmed that the IC’s tested did in fact operate as expected with the proper logic levels being output. The hypotheses regarding the XOR gate involving floating inputs was verified and proven correct, as well as the correct operation and design of a 1-bit full adder. With the above information collected it is possible to build further designs including larger adders up to as many bits as one could want. The lab also provided a better understanding of how logic levels relate to actual input and output voltages and at which point the IC’s switch between logic-1 and logic-0 at the threshold voltage. The purpose of this lab was completed and it was a success.